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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/440,595	11/15/1999	NAVEED MAJID	PHA-23843	3147

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
PAREKH, NITIN	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/440,595	MAJID ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11-18-03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takagi et al. (US Pat. 6130458) in view of Lauffer et al. (IDS-paper #4, European Pat. 0471938A1), Wenzel et al. (US Pat. 6150724) and Pogge et al. (US Pat. 5998868).

Regarding claim 1, Takagi et al. disclose a multichip hybrid integrate circuit (IC)/module comprising:

- a power semiconductor chip (200 in Fig. 12A and B) and a control semiconductor chip (100 in Fig. 12A and B) comprising silicon-on-insulator (SOI) devices, and
- the power and control semiconductor chips being directly mounted on an electrically conductive substrate connected to ground potential without using a separate insulating layer (81 in Fig. 12B)

(Fig. 12A and B; Fig. 15; Col. 11, line 30-Col. 12, line 57).

Takagi et al. fail to specify:

a) the control semiconductor chip comprising a bulk technology device, and

b) the substrate being a heat sink substrate.

a) Lauffer et al. teach using a multichip module (Fig. 4; Col. 12 and 13) having a variety of chips such as memory chip, logic/control chip, high power/low power, etc. where the chips such as logic/control chip (115 in Fig. 4) comprising conventional bulk technology is used in combination with the other chips in the same package (Col. 13, line 5-42).

Wenzel et al. teach using a multichip module (Fig. 5-8) having a chip/mother chip being connected to a single or multilayer conductor substrate having no insulating layer between the device/device layer and the substrate (106a in Fig. 5-8; Col. 5, line 63), the substrate having a heat sink structure for improved heat dissipation (Col. 7, line 50- Col. 8, line 10). Wenzel et al further teach selecting the chip from a variety of configurations and technology types such as DRAM, SRAM, EPROM, microprocessor control unit (MCU), CPU, power/MOSFET device, analog/digital sensor, etc. made from any of the material/technology such as silicon, SOI, etc. (Col. 6, line 60- Col. 7, line 25).

Pogge et al. teach using a variety of configurations of a multichip/very dense hybrid module (see Fig. 7 and Fig. 10) where the chips comprising different type/technology and functions applications including DRAM, SRAM, FLASH, MCU, logic/control, etc (Col. 4, line 35-52; Col. 11, line 10-25; Col. 13, line 27-35) can be directly mounted on a single substrate/carrier (700 and substrate CS in Fig. 7 and 10A/B respectively) without any additional insulating layer to improve chip density/yield and power requirements (Col. 4, line 30-35). Pogge et al further teach using the chips which can be combined in mix and match approach such that the chips can have similar or dissimilar technology types such as silicon, SOI, GaAs, etc (Col. 11, line 10-25; Col. 14, line 40-45).

b) Lauffer et al. teach using a multichip module having a variety of chips such as high power, low power, memory, logic chip, etc. in the same package being directly mounted on the electrically conductive heat sink/substrate made of copper (11 in Fig. 4; Col. 9, line 7) which is connected to a ground potential (Col. 12, line 32).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a control semiconductor chip comprising a bulk technology device and an electrically conductive heat sink substrate connected to ground potential as taught by Lauffer et al., Wenzel et al. and Pogge et al. so that heat dissipation, temperature distribution and power requirement can be improved in Takagi et al's multichip module.

Regarding claims 2-4, Takagi et al., Lauffer et al., Wenzel et al. and Pogge et al. teach substantially the entire claimed structure as applied to claim 1 above, and Takagi et al. further teach the control semiconductor chip comprising CMOS or any other configurations comprising BICMOS, bipolar, n-MOS, etc. (Col. 13, line 64).

Regarding claim 5, Takagi et al., Lauffer et al., Wenzel et al. and Pogge et al. teach substantially the entire claimed structure as applied to claim 1 above, except the substrate being a heat sink substrate.

As explained above for claim 1, Lauffer et al. teach using a multichip module having a variety of chips such as high power, low power, memory, logic chip, etc. in the same package being directly mounted on the electrically conductive heat sink/substrate

made of copper (11 in Fig. 4; Col. 9, line 7), which is connected to a ground potential (Col. 12, line 32).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a control semiconductor chip comprising a bulk technology device and an electrically conductive heat sink substrate being connected to ground potential as taught by Lauffer et al. so that heat dissipation, temperature distribution and power requirement can be improved in Wenzel et al., Pogge et al. and Takagi et al's multichip module.

Regarding claims 6 and 7, Takagi et al., Lauffer et al., Wenzel et al. and Pogge et al. teach substantially the entire claimed structure as applied to claim 1 above, except the heat sink comprising a metal or copper respectively.

As explained above for claim 1, Lauffer et al teach using a multichip module having a variety of chips such as high power, low power, memory, logic chip, etc. in the same package being directly mounted on the electrically conductive heat sink/substrate made of copper (11 in Fig. 4; Col. 9, line 7) which is connected to a ground potential (Col. 12, line 32).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a control semiconductor chip comprising a bulk technology device and an electrically conductive heat sink comprising copper metal as taught by Lauffer et al. so that heat dissipation, temperature distribution and power requirement can be improved in Wenzel et al., Pogge et al. and Takagi et al's multichip module.

Response to Arguments

3. Applicant's arguments filed on 06-13-03 have been fully considered but they are not persuasive.

A. Applicant contends that Takagi et al. is concerned only with the problems of SOI devices and the combination of Takagi et al. with other references is not proper.

However, as explained above, Wenzel et al. teach selecting one or more chips in the MCM from a variety of configurations and technology types such as DRAM, SRAM, EPROM, microprocessor control unit (MCU), CPU, power/MOSFET device, analog/digital sensor, etc. made from different material and technology/processes including silicon, SOI, etc. (Col. 6, line 60- Col. 7, line 25).

Pogge et al. teach using a variety of configurations of a multichip/very dense hybrid module where the chips comprising different type/technology and functions applications including DRAM, SRAM, FLASH, MCU, logic/control, etc (Col. 4, line 35-52; Col. 11, line 10-25; Col. 13, line 27-35) can be directly mounted on a single substrate/carrier without any additional insulating layer to improve chip density/yield and power requirement (Col. 4, line 30-35), such chips can be combined in mix and match approach having similar or dissimilar material and processes/technology types including silicon, SOI, GaAs, etc. (Col. 11, line 10-25; Col. 14, line 40-45).

Therefore, Wenzel et al. and Pogge et al's teachings are applied to improve chip density/yield and power requirement in Takagi's MCM.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Nitin Parekh
08-28-03